
13. Circuit Operating Descriptions

13-1 Power

13-1-1 About S.M.P.S (Ringing Choke Converter Method)

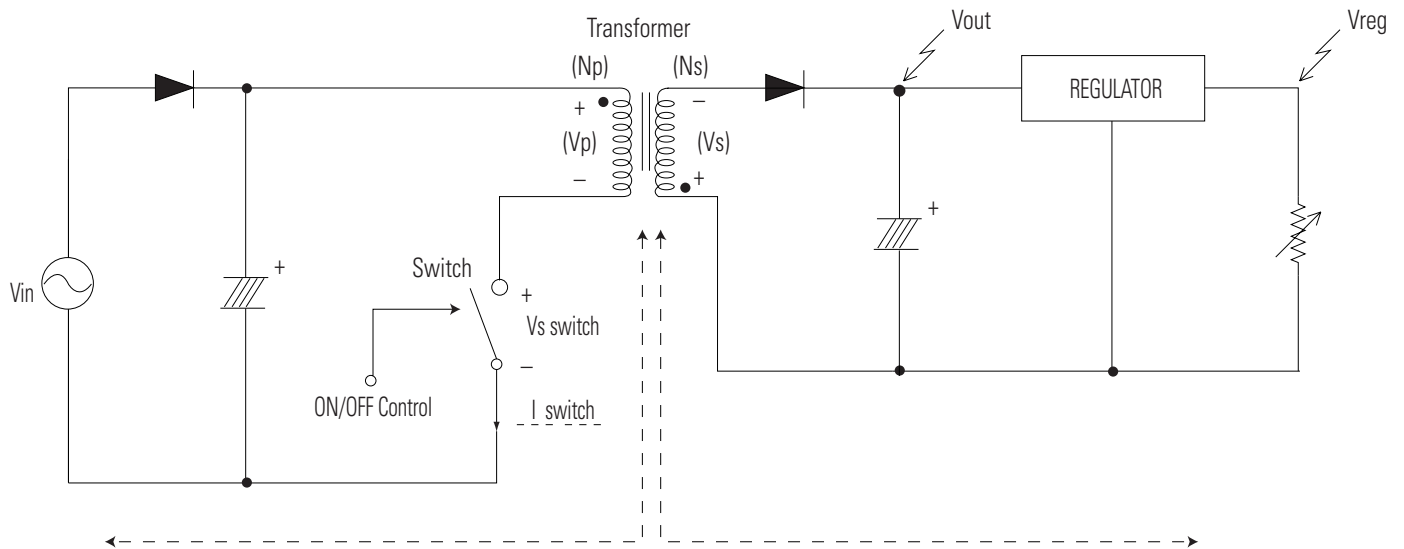


Fig. 13-1

◆Terms

- 1) 1st : Common power input to 1st winding.
- 2) 2nd : Circuit followings output winding of transformer.
- 3) f (Frequency) : Switching frequency (T : Switching cycle)
- 4) Duty : $(T_{on}/T) \times 100$

13-1-2 Circuit description [FLY-Back RCC(Ringing Choke Converter)] Control

(a) AC Power Rectification/Smoothing Terminal

- 1) PADT1, PADT2, PADT3, PADT4 : Convert AC power to DC (Wave rectification).
- 2) PRCU1 : Smooth the voltage converted to DC.
- 3) PALT1, PALT2, PACT1, PACT2 : Noise removal at power input/output.
- 4) PLRU1 : Rush current limit resistance at the momemt of power cord insertion.
 - Without PLRT1, the bridge diode might be damaged as the rush current increases.

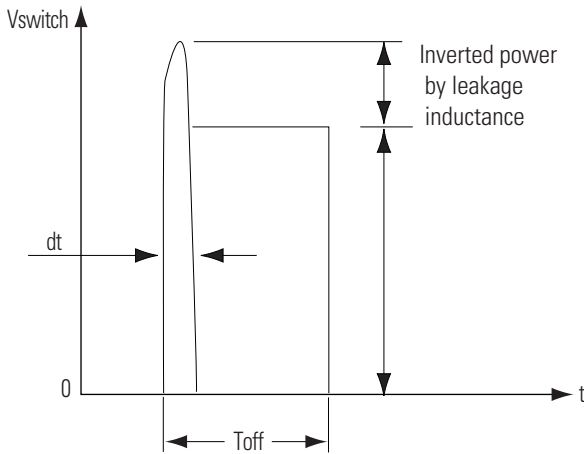


Fig. 13-2

(b) SNUBBER Circuit :

PSRZ1, PSRZ2, PSCX1, PSCZ2, PSDZ1

- 1) Prevent residual high voltage at the terminals of switch during switch off/Suppress noise. High inverted power occurs at switch off, because of the 1st winding of transformer :
 $(V = -L1 \times di/dt)$ $L1$: Leakage Induction
 A very high residual voltage exist on both terminals of PQIZ1 because dt is a very short.
- 2) SNUBBER circuit protects PQIZ1 from damage through leakage voltage suppression by RC, (Charges the leakage voltage to PSDZ1 and PSCX1 and discharges to PSRZ1, PSRZ2).
- 3) PSCZ2 : For noise removal

(c) PQIZ1 Vcc circuit

1) PQIZ1 Vcc : PVRL4, PVDL1, PVCL1

- ① Use the output of transformer as Vcc, because the current starts to flow into transformer while PQIZ1 is active
- ② Rectify to PVDL1 and smooth to PVCL1.
- ③ Use the output of transformer as PQIZ1 Vcc : The loads are different before and after PQIZ1 driving.
 (Vcc of PQIZ1 decreases below OFF voltage , using only the resistance due to load increase after PQIZ1 driving.)

(d) Feedback Control Circuit

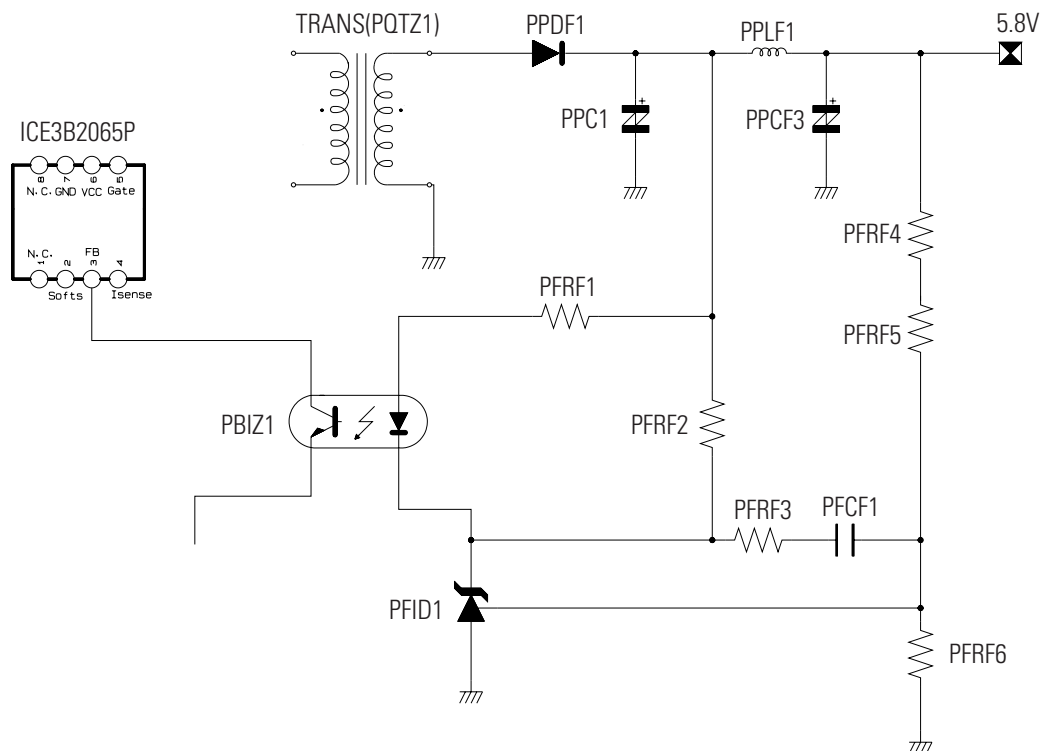


Fig. 13-3

- 1) F/B terminal of PQIZ1 determines output duty cycle.
- 2) C-E (Collector-Emitter) of PQIZ1 and F/B potential of PQIZ1 are same.

13-1-3 Internal Block Diagram (Internal Block Diagram of S.M.P.S. Circuit)

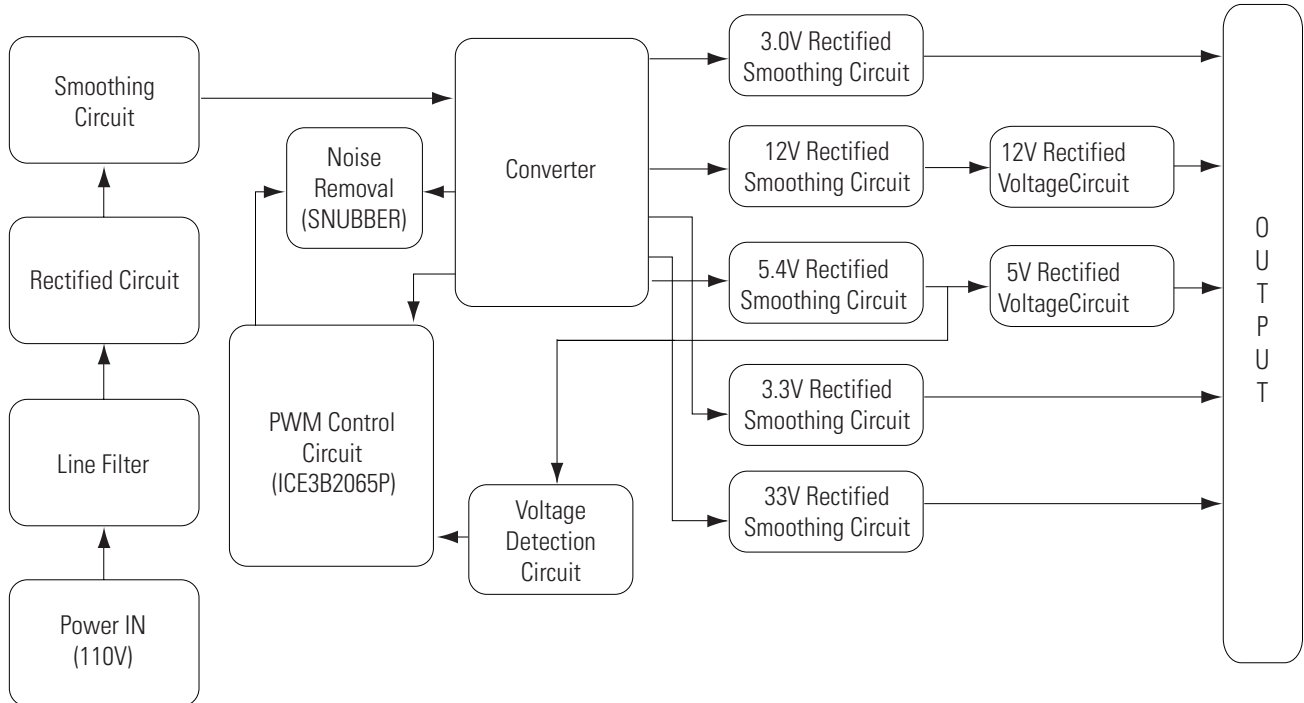


Fig. 13-4

13-2 AV Codec

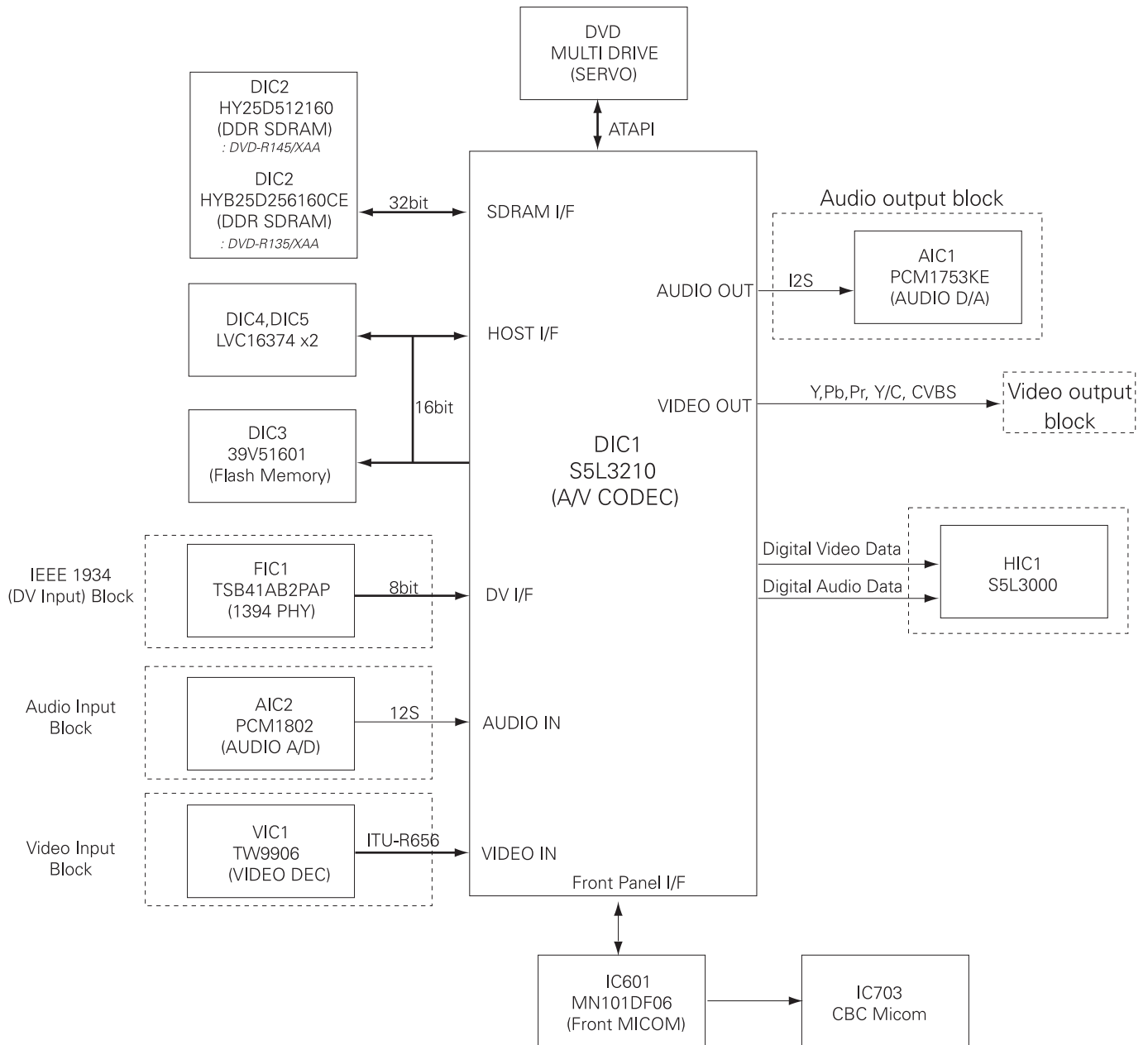


Fig. 13-5

- Main system control
- A/V Encoding/Decoding
- Transcoding/rating
- IEEE 1394 link layer function
- ATAPI interface with DVD-Multi Drive
- Analog Progressive/interlaced video output

13-2-1 GENERAL DESCRIPTION

SAMSUNG S5L3210 MPEG AV Codec is designed to provide a cost-effective, low power and high performance DVD recorder solution for DVD-VR, DVD-Video, DVD-Audio & many of CD applications. To reduce total system cost, S5L3210 also provides the following features: a front-end controller, a back-end decoder, a control CPU with separate 4KB Instruction and 4KB Data Cache, improved audio DSPs, a programmable video encoder with a dual output capability of interlaced and progressive scan, a DDR memory controller, 4-channel Timers with PWM, I/O Ports, 6-channel 10-bit Video DACs, 2-channel PWM processors for Hi-fi Audio, 2-channel UARTs with hand-shake, IIC-BUS interface, IIS interface, SPI, ATAPI, IEEE1394, USB 2.0 Full & Low Speed Host I/F and PLL for clock generation.

13-2-2 A/V Processor (DIC1) Functional Description

1) RISC processor architecture

- ARM946ES Core processor
- Fully 16/32-bit RISC architecture.
- Harvard cache architecture with separate 4KB Instruction and 4KB Data cache
- Protection unit to partition memory and set individual protection attributes for each partition
- Up to 160 MHz operating frequency

2) Memory controller

- Address space: 128M bytes for each bank (Total 1Gbyte space)
- Supports programmable 8/16-bit data bus width for ROM/SRAM interface.
- Supports 16-bit data bus width for DDR-SDRAM interface.
- 3 memory banks. - 2 memory banks for ROM, SRAM etc. - 1 memory banks for SDRAM
- Fully Programmable access cycles for all memory banks.
- Supports external wait signal to expand the bus cycle.

3) Cache memory

- 64 way set-associative cache with I-Cache (4KB) and D-Cache (4KB).
- 8-words per line with one valid bit and two dirty bits per line
- Pseudo random or round robin replacement algorithm.
- Write through or write back cache operation to update the main memory.
- The write buffer can hold 8 words of data and four address.

4) Clock & power manager

- Low power consumption
- On-chip PLLs
- Clock can be fed selectively to each function block by software.

5) **Interrupt controller**

- 62 interrupt sources(Watch dog timer, 4 Timers, UARTs, 8 External interrupts, IIC, IIS, SPI, IR,...)
- Edge detect mode on external interrupt source.
- Programmable polarity of rising and falling.
- Supports FIQ (Fast Interrupt request) for very urgent interrupt request.

6) **Video pre-processor**

- Noise Reduction by Motion-compensated Temporal Filtering.
- Bitmap Generation for Motion Estimation of MPEG Encoder.
- Scene Change Detection.

7) **MPEG video encoder**

- Encodes MPEG1 & MPEG2 video stream (MP@ML)
- Efficient Motion Estimation by reduced calculation and accurate Motion Vector Search

8) **MPEG video decoder**

- Decodes MPEG1, MPEG2 (MP@ML) & DivX/MPEG4 video stream(ASP)
- Error detection and autonomous error concealment.

9) **Audio DSP**

- Decodes Dolby AC-3, MPEG1, MPEG2, DTS and WMA
- Supports down mix
- MAC2424 for audio signal processing
 - 24-bit high performance fixed-point DSP coprocessor, 24x24 MAC operation in 1 cycle
 - 2 multiplier accumulator registers, 4 general accumulator registers, and 8 pointer registers

13-3 SERVO (DVP Multi Drive)

1) Pick-Up

Data in the disc is processed from the optical pick-up unit (OPU). OPU includes the Elantec chip (EL6912c) which is a highly integrated laser diode driver designed to support multi-standard writable optical drives. This chip also has an IV amplifier with concurrent read and write sampling. The architecture allows reprogramming of the timers to support different media DVD or CD standards, and different speed.

2) A-Chip

A chip is RF processor. This module performs RF signal processing which includes RFIP, RFIN, AGC, RF equalizer. This processor is able to detect tracking error, focus error and various signals such as CE, PE, SBAD, DEFECT, BCA, MIRROR, Wobble, TZC, RC, and RECD.

3) C-Chip

C-Chip is composed of DP1, PRML and WS.

First, the Data processor1 (DP1) performs EFM/EFM+ Demodulation and data is stored in the buffer memory in data processor2 (DP2). DVD data in this buffer is transferred to CSS/ATAPI through error-correction code

(ECC), descramble process and error detection code (EDC).

Second, WS performs the following processes.

- ① Delay compensation using Shift register
- ② Sample/Hold pulse generation
- ③ I/V Gain Control
- ④ Providing clock for RF chip
- ⑤ OPC Control signal generation

Lastly, PRML completes the adaptive EQ/VD and Digital PLL.

4) D-Chip

D-Chip consists of Servo DSP, DP2 and 1Mbit memory. Servo DSP is dealing with controlling the servo-mechanism in DVD recorder. Servo-DSP has the following features.

- ① Built-in 10Bit ADC(8ch), DAC(3ch) and PWM(7ch)
- ② Step Motor Control Logic: Macro/Micro Step
- ③ Track Counter: long distance velocity control direct seek
- ④ Shock/Defect detection
- ⑤ Header (DVD-RAM)/Land Pre-Pit (DVD-R/RW) Detection
- ⑥ Several Servo Monitor Signal Detection
- ⑦ RF IC Interface
- ⑧ Micom Interface
- ⑨ Digital Servo Control of focus, tracking, sled and seek
- ⑩ Disc Auto-Detection
- ⑪ Automatic Adjustment of the offset, balance and gain of Focus and Tracking Signal
- ⑫ Direct Seek with Velocity Control
- ⑬ Step Motor Control: Macro Seek
- ⑭ De-Track and Lens Shift Detection and Compensation
- ⑮ Center Error Control
- ⑯ DVD Layer Jump
- ⑰ Tilt Detect and Compensation

DP2 performs High Speed ECC and CD DA Decoder.

5) ATAPI Controller

ATAPI (ATA Packet Interface) the standard interface protocol used to connect the CD/DVD Drive to IDE interface. Data from the front-end is processed to back-end through this ATAPI protocol. Sanyo chip (LC98600CT-XB0) is utilized for ATAPI interface. LC98600CT-XB0 has the following features.

- ① ECC and EDC correction/addition for CD-ROM data
- ② Subcode decoding/encoding
- ③ Spindle servo control
- ④ CLV/CAV servo control using ATIP data
- ⑤ ATIP decoding and CRC check functions
- ⑥ Providing random EFM output for PCA use
- ⑦ High-accuracy write strategy signal output enabled (CD-R 52x)
- ⑧ Buffer RAM can be accessed by the microcontroller through the LC98600CT-XB0
- ⑨ Built-in ATA-PI(IDE) interface (supports Ultra DMA modes 0,1, and 2)
- ⑩ 52x decoding speed/52x encoding speed supported with 33.8688Mhz
- ⑪ Maximum transfer speed PIO mode: 16.6 MB/s (with IORDY), Ultra-DMA: 66MB/s (with DMARQ)
- ⑫ User can freely set the CD main channel, C2 flag, and subcode areas in buffer RAM
- ⑬ Built-in batch transfer function for transferring (CD main channel, C2 flag, etc., in a single operation)
- ⑭ Built-in multi-transfer function (allows multiple blocks to be sent to the host automatically in a single operation)

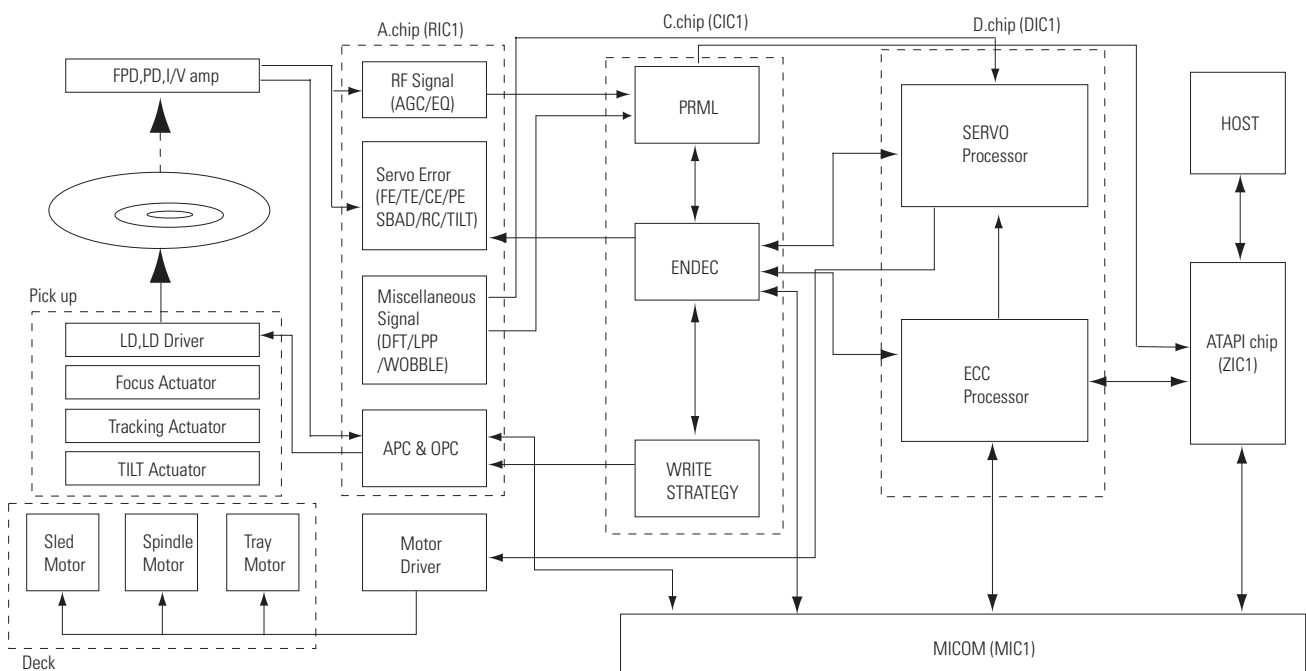


Fig. 13-6

13-4 Video Input

13-4-1 Video Input Outline

The model specified in this book uses service manual is the two AV Video input. AV 1 Video input is CVBS1 & S-Video1 at the Rear Panel. AV 2 Video input is CVBS2 at the Front Panel.

The analog Video signal select AV 1 or AV 2 by the IC601 (Front Micom).

TIC1 (Video Decoder) diverges from the 27MHz crystal, then generates ITU-R656 (10bits) and 27MHz clock. VIC1 (Video Decoder) does closed caption, copy guard detect processing and A/D conversion of analog Video signal converted into 11bit Digital Video signal (ITU-R656 Format) is outputted via DIC1 (MPEG2 Decoder & Encoder with video Encoder) of digital part.

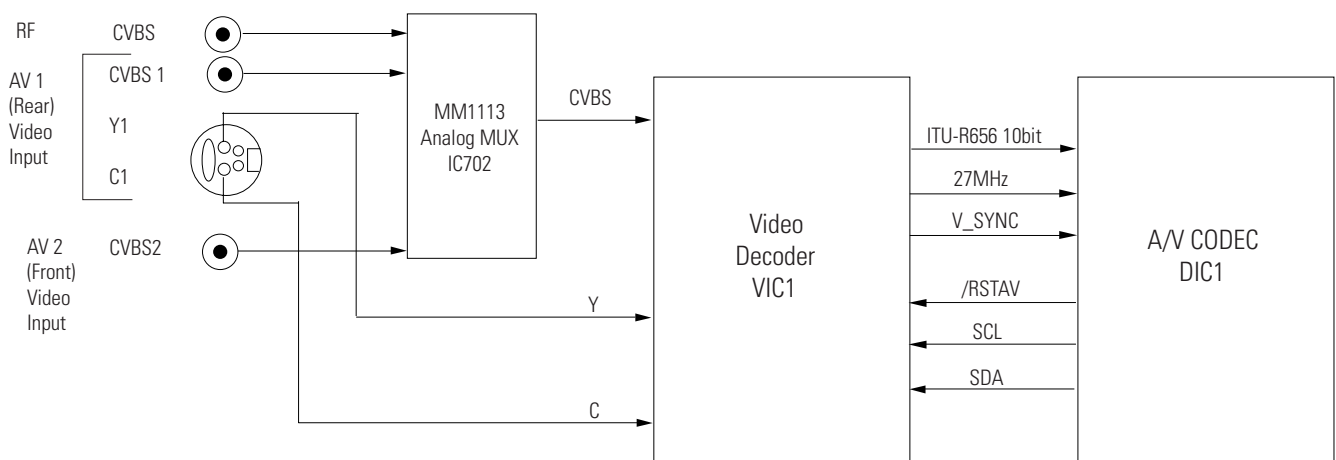


Fig. 13-7

13-4-2 Analog Mux (MM1113)

IC702 is Analog Mux.

As Pin 2, 4 of the IC702 are controlled by the Front Micom, IC702 select RF OF CVBS(Pin1)

Line1 of CVBS[Pin3] and AV2 of CVBS[Pin 5].

The analog Video Signal of IC201 output is selected by the IC601 via VIC1(Video Decoder : TW9906) of analog Video Input parts.

13-4-3 NTSC/PAL Video Decoder (TW9906 : Video Decoder)

The VIC1 (Video Decoder : TW9906) device is a high quality, single-chip digital video decoder that digitizes and decodes all popular baseband analog video formats into digital component video. The VIC1 (Video Decoder : TW9906) supports the analog-to-digital (A/D) conversion of component RGB and YPbPr signals, as well as the A/D conversion and decoding of NTSC, PAL and SECAM composite and S-video into component YCbCr. This VIC1 (Video Decoder : TW9906) includes four 10-bit 30-MSPS A/D converters. and A/D conversion of 10bit analog Video signal converted into Digital Video signal (ITU-R656 Format) is outputted via DIC1 (MPEG2 Decoder & Encoder with video Encoder) of digital part.

The following output formats supply 10-bit 4:2:2 YCbCr to the DIC1 (MPEG2 Decoder & Encoder with video Encoder) of digital part.

On CVBS and S-video inputs, the user can control video characteristics such as contrast, Brightness, saturation, and hue via an I2C DIC1 port [PIN V17, V18] interface.

The TW9906 decoder includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor (VDP) slices, parses, and performs error checking on teletext, closed caption (CC), Copy Guard Detect Processing and other VBI data.

13-5 Video Output

13-5-1 Outline

DIC1 (MPEG2 Decoder & Encoder with video Encoder) diverges from the 13.5MHz crystal, then generates VSYNC and HSYNC.

DIC1 (MPEG2 Decoder & Encoder with video Encoder) does RGB encoding, copy guard processing and D/A conversion of 10bit Video signal converted into analog signal is outputted via amplifier of analog part.

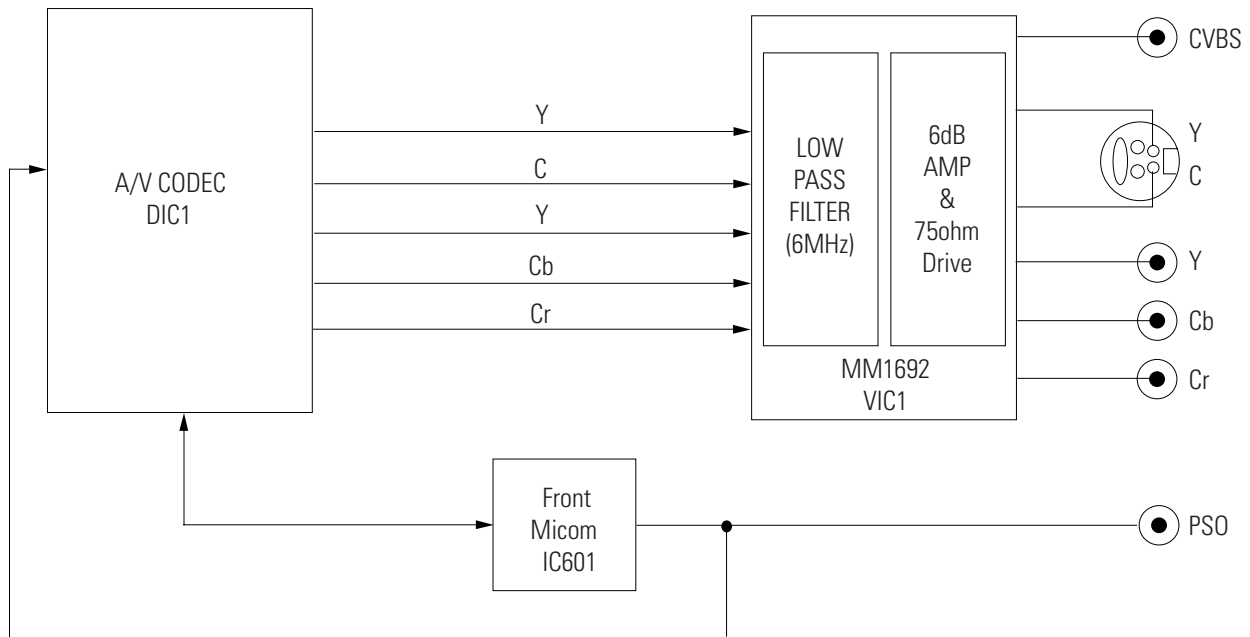


Fig. 13-8

13-5-2 NTSC/PAL Digital

DIC1 inputted from pin E1 with 13.5MHz generates HSYNC and VSYNC which are based on video signal. DIC1 is synchronous signals with decoded video signal.

The above signals, which are CVBS (Composite Video Burst Synchronized), Y(S_Video), C(S_Video), Y(Component)/G(Green), Cr(component)/R(Red), Cb(component)/B(Blue), are selectively outputted 480I(interlaced Video Output), 480P(progressive Video Output) by the Pront button DIC1 adopts 10bit D/A converter. DIC1 perform video en-coding as well as copy protection.

13-5-3 Amplifier (MM1692)

VIC1 of JACK PCB is 6dB amplifier.

Based on CVBS signal, the final output level must be 2Vpp without 75ohm terminal resistance. Because the level of video encoder output is only 1Vpp, the level is adjusted with the special amplifier.

When mute of pin 5 is high active, if the pin is floating and connect to power, the output signal is never outputted.

Y, C, Y(R), Cb(B), Cr(R) outputted from video encoder are inputted to VIC1 [Pin14, 16, 13, 12, 11] respectively. And CVBS Output[Pin 15] is made by Y & C Mixing signal.

The signal to which gain is adjusted by amplifier is outputted from jack via 75ohm Resistance (VDR1,2,4,5,6,).

13-6 Audio

13-6-1 Input Block

This Model has two stereo line input terminals, and internal TV-audio from RF Tuner Block.

These three Analog audio signal source are converted to digital data by Input Block.

Input Block has a Multiplexer (IC203), A/D converter (AIC2).

IC203 change it's output by selection control signal from IC601 (Front Micom).

13-6-2 Output Block

The model specified in this book uses service manual has two stereo analog line out terminal, and two digital output terminal.

Decoded signal by DIC1 is inputted to AIC1 (D/A Converter), then filtered and amplified by AIC4 (OP-Amp).

And the digital audio signal (IEC-958) is outputted in Optical/Coaxial (S/PDIF) terminal.

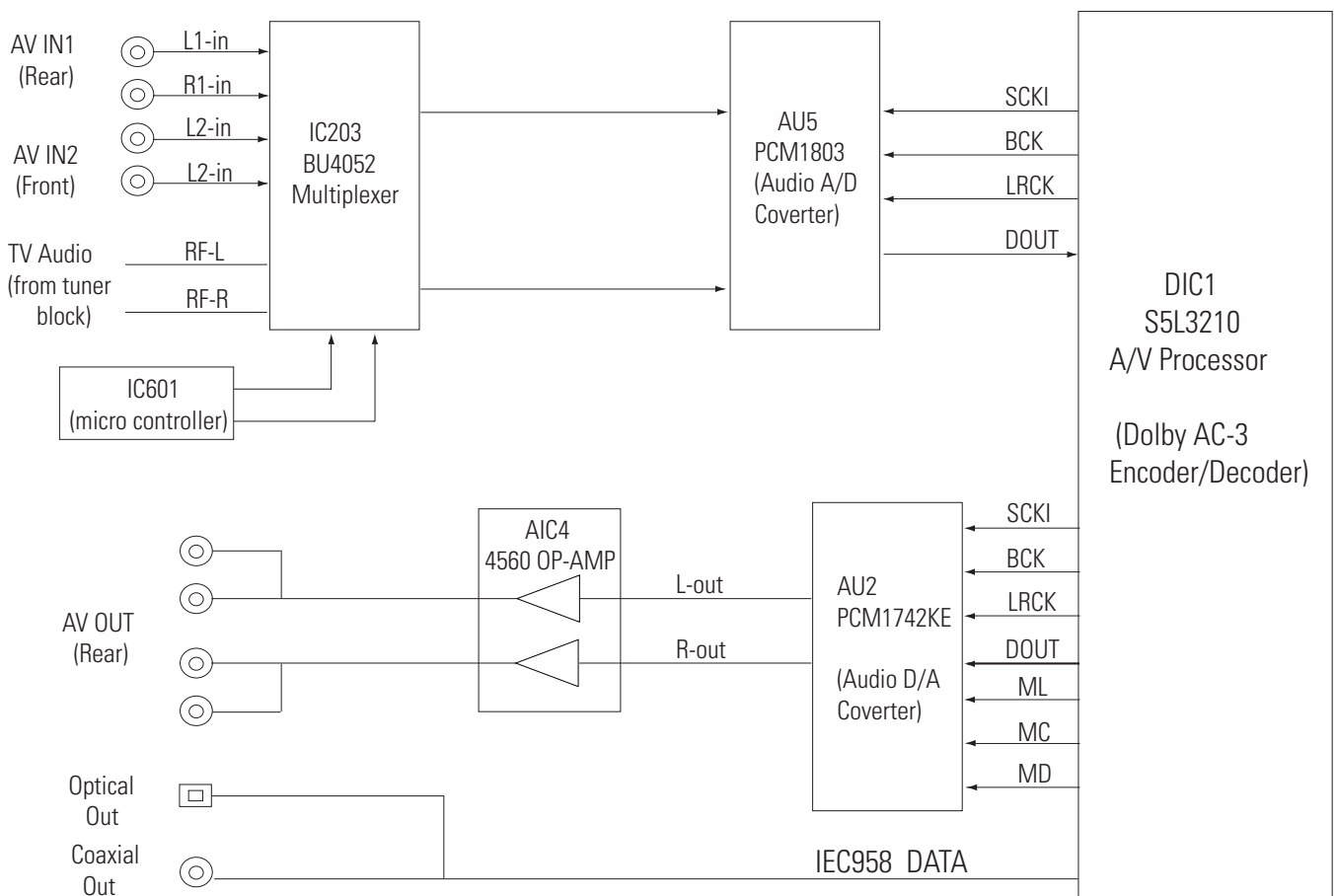


Fig. 13-9

13-7 Tuner

1) Low Pass Filter & High Pass Filter

This consists of IF trap circuit and UHF & VHF separation circuit. If the input signal is IF (45.75MHz), this filter prevents interference.

2) Single tune

This consists of a filter circuit, RF AMF, impedance conversion circuit, image trap and a single tuning circuit. It prevents noise and other interference signals. It is very important part which improves NF (noise figure) and prevents the various of spurious signals.

3) RF AMF

RF AMF is made of FET (Field Effects Transistor). It is controlled by AGC coming from IF DEMOD block.

4) Double tune

It consists of a double tuning circuit to improve characteristic of rejection that results in a better band characteristic.

5) Mixer IC (Mixer, OSC, PLL)

It consists a VHF and UHF OSC and Mixer circuit. We applied mixer to make better characteristic of rejection, it shows especially various beat characteristic.

6) PLL IC

The PLL IC plays a role selection of Tuner channel. It was built-in three wire PLL IC, charge pump and band driver.

The minimum of step frequency is 31.25KH z.

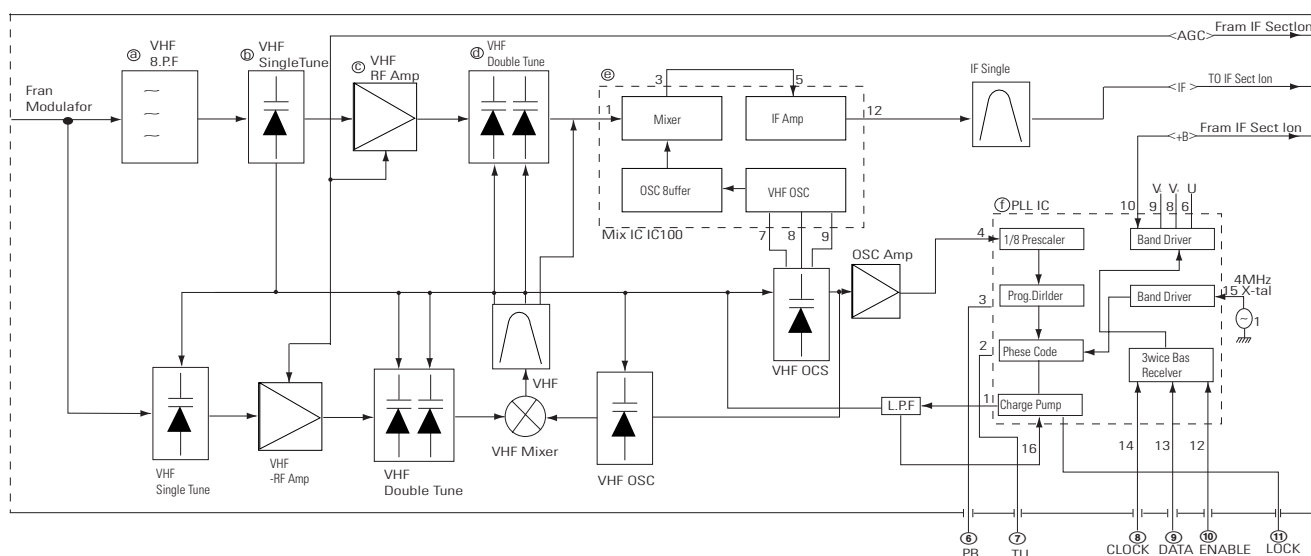


Fig.13-10

13-8 IF

1) SAW FILTER

It passes only needed band of the signal that is converted to IF frequency and decrease the others band to minimize the effect of adjacent channel.

2) RF AGC Control

It used adjusting to determine RF AGC working point in tuner.

3) VCO Tank

When VCO tank detects PLL, it makes the signal which sets a standard.

4) AFT (Auto Frequency Tuning)

AFT automatically controls the oscillator frequency in the tuner, so that it retains a constant level.

It is a quadrature detection type. The carrier, which is detected from video det is directly input to AFT.

The 90 degree delayed phase signal is input at the same time to AFT and, the results come out.

5) IF AMP

IF signal, which is selected in Saw filter, is amplified in IF amp frequency enough to be detected. The IF amp has parallel inputs & outputs structure.

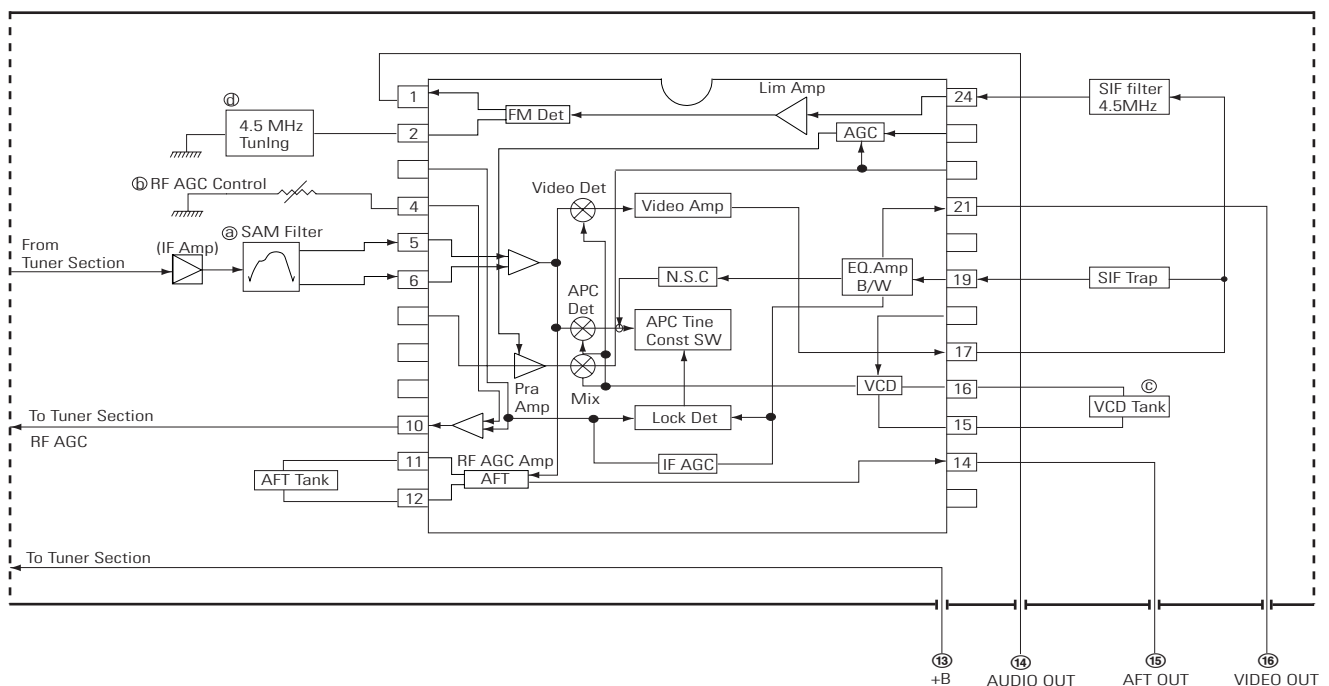


Fig. 13-11

MEMO